KNOWLEDGEINSTITUTEOFTECHNOLOGY

(An Autonomous Institution)

Approved by AICTE, Affiliated to Anna University, Chennai.
Accredited by NBA (CSE,ECE,EEE&MECH), Accredited by NAAC with "A" Grade
KIOT Campus, Kakapalayam (PO), Salem – 637 504, Tamil Nadu, India.

M.E.Regulations2023

M.E.–VLSI DESIGN

Curriculum and Syllabi

(For the Students Admitted from the Academic Year 2023 – 24 Onwards)

Version:1 .0	**Date:**09.09.2023

	KNOWLEDGE INSTITUTE OF TECHNOLOGY(AUTONOMOUS), SALEM -637504
	Approved by AICTE, Affiliated to Anna University, Accredited by NAAC and NBA (B.E.:Mech.,ECE,EEE&CSE)
	Website:www.kiot.ac.in

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M.E.REGULATIONS2023 (R2023)

CHOICEBASEDCREDITSYSTEMANDOUTCOMEBASEDEDUCATION

M.E. VLSI DESIGN

VISION OF THE INSTITUTE
To be a world class institution to impart value and need based professional education to the aspiring youth and carving them into disciplined world class professional who have the quest for excellence, achievement orientation and social responsibilities.

MISSIONOFTHEINSTITUTE	
A	To promote academic growth by offering state-of-art under graduate, post graduate, and doctoral programs and to generate new knowledge by engaging in cutting – edge research
B	To nurture talent, innovation, entrepreneurship, all-round personality, and value system among the students and to foster competitiveness among students
C	To undertake collaborative projects which offer opportunities for long-term interaction with academia and industry
D	To pursue global standards of excellence in all our endeavors namely teaching, research, consultancy, continuing education and support functions

VISIONOFTHEDEPARTMENT
To produce competent Electronics and Communication Engineers by imparting quality education to meet the industry requirements and for serving the societal needs

MISSIONOFTHEDEPARTMENT	
M1	To develop appropriate facilities for promoting research activities
M2	To inculcate leadership qualities among students for self and societal growth
M3	To nurture students on emerging technologies for serving industry needs through industry institute interface
M4	To enrich teaching learning process by transforming young minds to be resourceful engineers

PROGRAMEDUCATIONALOBJECTIVES(PEOs)	
PEO1	To critically analyze and understand the principles involved in the designing and testing of electronic circuits relevant to industry and society.
PEO2	To appreciate the concepts in the working of electronic circuits
PEO3	To take up socially relevant and challenging projects and to provide Innovative solutions through research for the benefit of the society with latest hardware & software related to VLSI and also to develop the capacity to protect Intellectual Property.
PEO4	To Progress and Develop with Ethics and Communicate effectively.
PEO5	To become entrepreneurs to develop indigenous solutions

PROGRAMOUTCOMES(POs)	
PO1	An ability to independently carry out research/investigation and development work to solve practical problems
PO2	An ability to write and present a substantial technical report/document
PO3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program
PO4	Understand the fundamentals involved in the Designing and Testing of electronic circuits in the VLSI domain.
PO5	Provide solutions through research to socially relevant issues for modern Electronic Design Automation (EDA) tools with knowledge, techniques, skills and for the benefit of the society
PO6	Interact effectively with the technical experts in industry

PROGRAM SPECIFICOUTCOMES(PSOs)	
	Upon completion of the Post Graduate Engineering program in VLSI Design
PSO1	Students will be able to demonstrate advanced proficiency in designing and optimizing VLSI circuits, applying their knowledge to create efficient, high-performance electronic systems
PSO3	Students will exhibit a deep understanding of emerging trends and technologies in VLSI design, enabling them to contribute for research and development in the field

KNOWLEDGEINSTITUTEOFTECHNOLOGY(AUTONOMOUS), SALEM-637504											
M.E. VLSI DESIGN											Version:1.0
Courses of Study and Scheme of Assessment (Regulations2023)											Date:09.09.23
Sl. No.	Course Code	Course Title	Periods/ Week						Maximum Marks		
			CAT	CP	L	T	P	C	IA	ESE	Total
	SEMESTERI										
	THEORY										
1	ME23MA102	Graph Theory and Optimization Techniques	FC	4	3	1	0	4	40	60	100
2	ME23RM201	Research Methodology and IPR	RM	3	3	0	0	3	40	60	100
3	ME23VL301	Analog IC Design	PC	3	3	0	0	3	40	60	100
4	ME23VL302	Digital CMOS VLSI Design	PC	3	3	0	0	3	40	60	100
5	ME23VL303	Advanced Digital System Design	PC	3	3	0	0	3	40	60	100
6	ME23VL304	RFIC Design	PC	3	3	0	0	3	40	60	100
7	ME23VL801	Technical Seminar / Case study presentation	PT	2	0	0	2	1	100	-	100
8	ME23VL7XX	Audit Course – I	AC	2	2	0	0	0	100	-	100
	PRACTICAL										
8	ME23VL305	FPGA Laboratory	PC	4	0	0	4	2	60	40	100
9	ME23VL306	Analog IC Design Laboratory	PC	4	0	0	4	2	60	40	100
Total				29	18	1	10	24	480	420	900

SEMESTER II											
Sl. No.	Course Code	Course Title	Periods / Week						Maximum Marks		
			CAT	CP	L	T	P	C	IA	ESE	Total
THEORY											
1	ME23VL307	Design for Verification using UVM	PC	3	3	0	0	3	40	60	100
2	ME23VL308	Low Power VLSI Design	PC	3	3	0	0	3	40	60	100
3	ME23VL309	VLSI Testing	PC	3	3	0	0	3	40	60	100
4	ME23VL4XX	Professional Elective –Sem II	PE	3	3	0	0	3	40	60	100
5	ME23VL4XX	Professional Elective –Sem II	PE	3	3	0	0	3	40	60	100
6	ME23VL5XX	Open Elective - I	OE	3	3	0	0	3	40	60	100
7	ME23VL702	Universal Human Values and Professional Ethics	MC	3	3	0	0	3	40	60	100
8	ME23VL7XX	Audit Course – II*	AC	2	2	0	0	0	100	-	100
PRACTICAL											
9	ME23VL310	Verification using UVM Laboratory	PC	4	0	0	4	2	60	40	100
EMPLOYABILITY ENHANCEMENT											
10	ME23VL801	Research Paper Review and presentation	PT	2	0	0	2	1	60	40	100
		Total		27	21	0	6	24	400	500	900

SEMESTER III

Sl. No.	Course Code	Course Title	Periods / Week						Maximum Marks		
			CAT	CP	L	T	P	C	IA	ESE	Total
THEORY											
1	ME23VL311	VLSI Signal Processing	PC	3	3	0	0	3	40	60	100
2	ME23VL4XX	Professional Elective – Sem III	PE	3	3	0	0	3	40	60	100
3	ME23VL4XX	Professional Elective – Sem III	PE	3	3	0	0	3	40	60	100
4	ME23VL5XX	Open Elective - II	OE	3	3	0	0	3	40	60	100
PRACTICAL											
5	ME2**3**VL601	Project Work - I	PW	12	0	0	12	6	60	40	100
		Total		**24**	**12**	**0**	**12**	**18**	**220**	**280**	**500**

SEMESTER IV

Sl. No.	Course Code	Course Title	Periods / Week						Maximum Marks		
			CAT	CP	L	T	P	C	IA	ESE	Total
PRACTICAL											
1	ME2**3**VL602	Project Work - II	PW	24	0	0	24	12	60	40	100
		Total		**24**	**0**	**0**	**24**	**12**	**60**	**40**	**100**

NOMENCLATURE					
CAT	Category of Course	FC	Foundation Courses	PW	Project Work Courses
CP	Contact Period	RM	Research Methodology and IPR Courses	PT	Employability Enhancement Course
L	Lecture Period	PC	Professional Core Courses	AC	Audit Course
T	Tutorial Period	PE	Professional Elective Courses	IA	Internal Assessment
P	Laboratory Period	OE	Open Elective Courses	ESE	End Semester Examination
C	Credits	SE	Special Elective		

SEMESTER II
PROFESSIONAL ELECTIVES

Sl. No.	Course Code	Course Title	Periods / Week						Maximum Marks		
			CAT	CP	L	T	P	C	IA	ESE	Total
THEORY											
1.	ME23VL401	ASIC Design	PE	3	3	0	0	3	40	60	100
2.	ME23VL402	Medical Imaging Systems	PE	3	3	0	0	3	40	60	100
3.	ME23VL403	Principles of Sensors and Signal Conditioning	PE	3	3	0	0	3	40	60	100
4.	ME23VL404	Hardware Software Co-Design for FPGA	PE	3	3	0	0	3	40	60	100
5.	ME23VL405	DSP Structures for VLSI	PE	3	3	0	0	3	40	60	100
6.	ME23VL406	Power Management and Clock Distribution Circuits	PE	3	3	0	0	3	40	60	100
7.	ME23VL407	Reconfigurable Architectures	PE	3	3	0	0	3	40	60	100
8.	ME23VL408	Advanced Wireless Sensor Networks	PE	3	3	0	0	3	40	60	100
9.	ME23VL409	Edge and Fog Computing	PE	3	3	0	0	3	40	60	100
10.	ME23VL410	System On Chip	PE	3	3	0	0	3	40	60	100

SEMESTER III

PROFESSIONAL ELECTIVES

Sl. No.	Course Code	Course Title	Periods / Week						Maximum Marks		
			CAT	CP	L	T	P	C	IA	ESE	Total
THEORY											
1.	ME23VL411	MEMS and NEMS	PE	3	3	0	0	3	40	60	100
2.	ME23VL412	Network on Chip	PE	3	3	0	0	3	40	60	100
3.	ME23VL413	Evolvable Hardware	PE	3	3	0	0	3	40	60	100
4.	ME23VL414	Soft Computing and Optimization Techniques	PE	3	3	0	0	3	40	60	100
5.	ME23VL415	CAD for VLSI Design	PE	3	3	0	0	3	40	60	100
6.	ME23VL416	VLSI Architectures for Image Processing	PE	3	3	0	0	3	40	60	100
7.	ME23VL417	System Verilog	PE	3	3	0	0	3	40	60	100
8.	ME23VL418	Adaptive Signal Processing	PE	3	3	0	0	3	40	60	100
9.	ME23VL419	Machine Learning	PE	3	3	0	0	3	40	60	100
10.	ME23VL420	Advanced Digital Image Processing	PE	3	3	0	0	3	40	60	100

OPEN ELECTIVES				
		Course Title	**Periods / Week**	**Maximum Marks**

S. No.	Course Code		CAT	CP	L	T	P	C	CIA	ESE	Total
Except M.E. Computer Science and Engineering											
1	ME23CP501	Security Practices	OE	3	3	0	0	3	60	40	100
2	ME23CP502	Cloud Computing Technologies	OE	3	3	0	0	3	60	40	100
3	ME23CP503	Blockchain Technologies	OE	3	3	0	0	3	60	40	100
4	ME23CP504	Deep Learning	OE	3	3	0	0	3	60	40	100
5	ME23CP505	Design Thinking	OE	3	3	0	0	3	60	40	100
6	ME23CP506	Principles of Multimedia	OE	3	3	0	0	3	60	40	100
Except M.E. Industrial Safety Engineering											
7	ME23IS501	Environmental Safety	OE	3	3	0	0	3	60	40	100
8	ME23IS502	Electrical safety	OE	3	3	0	0	3	60	40	100
9	ME23IS503	Safety in Engineering Industry	OE	3	3	0	0	3	60	40	100
10	ME23IS504	Design of Experiments	OE	3	3	0	0	3	60	40	100
11	ME23IS505	Circular Economy	OE	3	3	0	0	3	60	40	100
Except M.E. Embedded System Technologies											
12	ME23ES501	IoT for Smart Systems	OE	3	3	0	0	3	60	40	100
13	ME23ES502	Machine Learning and Deep Learning	OE	3	3	0	0	3	60	40	100
14	ME23ES503	Renewable Energy Technology	OE	3	3	0	0	3	60	40	100
15	ME23ES504	Smart Grid	OE	3	3	0	0	3	60	40	100
Except M.E. VLSI Design											
16	ME23VL501	Big Data Analytics	OE	3	3	0	0	3	60	40	100
17	ME23VL502	Internet of Things and Cloud	OE	3	3	0	0	3	60	40	100
18	ME23VL503	Medical Robotics	OE	3	3	0	0	3	60	40	100
19	ME23VL504	Embedded Automation	OE	3	3	0	0	3	60	40	100

PROJECT WORK

Sl. No.	Course Code	Course Title	Periods / Week						Maximum Marks		
			CAT	CP	L	T	P	C	IA	ESE	Total
THEORY											
1.	ME23VL601	Project Work I	PW	12	0	0	12	6	60	40	100
2.	ME23VL602	Project Work II	PW	24	0	0	24	12	60	40	100

FOUNDATION COURSE AND RESEARCH METHODOLOGY

Sl. No.	Course Code	Course Title	Periods / Week						Maximum Marks		
			CAT	CP	L	T	P	C	IA	ESE	Total
THEORY											
1.	ME23MA102	Graph Theory and Optimization Techniques	FC	4	3	1	0	4	40	60	100
2.	ME23VL201	Research Methodology and IPR	RM	3	3	0	0	3	40	60	100

AUDIT COURSES (AC)

Registration for any of these courses is optional to students											
Sl. No.	**Course Code**	**Course Title**	**Periods / Week**						**Maximum Marks**		
			CAT	**CP**	**L**	**T**	**P**	**C**	**IA**	**ESE**	**Total**
THEORY											
1	ME23AC701	English for Research Paper Writing	AC	2	2	0	0	0	100	-	100
2	ME23AC702	Disaster Management	AC	2	2	0	0	0	100	-	100
3	ME23AC703	Constitution of India	AC	2	2	0	0	0	100	-	100
4	ME23AC704	நற்றமிழ் இலக்கியம்	AC	2	2	0	0	0	100	-	100

SUMMARY							
Sl. No.	**Course Category**	**Credits per Semester**				**Credits**	**Credit %**
		I	**II**	**III**	**IV**		
1	FC	4	-	-	-	4	5.12
2	RM	3	-	-	-	3	3.84
3	PC	16	11	3	-	30	38.46
4	PE	-	6	6	-	12	15.38
5	OE	-	3	3	-	06	7.69
6	PW	-		6	12	18	23.07
7	PT	✓ 1	1	-	-	02	2.56
8	MC	-	3	-	-	03	3.84
9	AC*	✓	✓	-	-	-	-
	Total	**24**	**24**	**18**	**12**	**78**	**100**

ME23MA102	GRAPH THEORY AND OPTIMIZATION TECHNIQUES	Version: 1.0				
Programme & Branch	M.E. VLSI DESIGN	CP	L	T	P	C
		4	3	1	0	4

Use of Calculator -fx991ms are permitted

Course Objectives:

1	To apply graph theory and models to solve connectivity problems.
2	To apply various graph algorithms for optimization.
3	To construct mathematical models for solving linear programming problems
4	To construct mathematical models for solving non-linear programming problems
5	To apply simulation modeling techniques for solving engineering problems.

UNIT–I	GRAPHS	9

Graphs and graph models – Graph terminology and special types of graphs – Matrix representation of graphs and graph isomorphism – Connectivity – Euler and Hamilton paths.

UNIT–II	GRAPH ALGORITHM	9

Graph Algorithms – Directed graphs – Some basic algorithms – Shortest path algorithms – Depth – First search on a graph – Theoretic algorithms – Performance of graph theoretic algorithms – Graph theoretic computer languages.

UNIT– III	LINEAR PROGRAMMING	9

Formulation – Graphical solution – Simplex method – Two-phase method – Transportation and Assignment Models.

UNIT – IV	NON-LINEAR PROGRAMMING	9

Constrained Problems – Equality constraints – Lagrangean Method – Inequality constraints – Karush – Kuhn-Tucker (KKT) conditions – Quadratic Programming.

UNIT–V	SIMULATION MODELLING	9

Monte Carlo Simulation – Types of Simulation – Elements of Discrete Event Simulation – Generation of Random Numbers – Applications to Queuing systems.

Total: 60 PERIODS

OPEN-ENDED PROBLEMS / QUESTIONS

Course specific Open Ended Problems will be solved during the class room teaching. Such problems can be given as Assignments and evaluated as Internal Assessment only and not for the End semester Examinations.

Course Outcomes: **Upon completion of this course the students will be able to:**		**BLOOM'S Taxonomy**
CO1	Apply graph theory and models to solve connectivity problems.	L3 - APPLY
CO2	Apply various graph algorithms for optimization.	L3 - APPLY
CO3	Construct mathematical models for solving linear programming problems	L3 - APPLY
CO4	Construct mathematical models for solving non-linear programming problems	L3 - APPLY
CO5	Apply simulation modeling techniques for solving engineering problems.	L3 - APPLY

REFERENCE BOOKS:

1.	Taha H.A, "Operation Research: An Introduction", Ninth Edition, Pearson Education, New Delhi, 2010.
2.	Gupta P. K, and Hira D.S., "Operation Research", Revise Edition, S. Chand and Company Ltd., 2012.
3.	Sharma J.K., "Operation Research", 3rd Edition, Macmillan Publishers India Ltd., 2009.
4.	Douglas B. West, "Introduction to Graph Theory", Pearson Education, New Delhi, 2015.
5.	Balakrishna R., Ranganathan. K., "A text book of Graph Theory", Springer Science and Business Media, New Delhi, 2012.
6.	Narasingh Deo, "Graph Theory with Applications to Engineering and Computer Science", Prentice Hall India,1997.
VIDEO REFERENCES:	
1.	https://youtube.com/playlist?list=PLEAYkSg4uSQ2fXcfrTGZdPuTmv98bnFY5
2.	https://youtube.com/playlist?list=PLU6SqdYcYsfLV24T0XVb3z3mjl8QG0EBN
WEB REFERENCES:	
1.	https://www.baeldung.com/cs/graph-theory-intro
2.	https://sitn.hms.harvard.edu/flash/2021/graph-theory-101/
ONLINE COURSES:	
1.	https://archive.nptel.ac.in/noc/courses/noc22/SEM1/noc22-ma10/
2.	https://www.udemy.com/course/graph-theory/

Mapping of COs with POs

COs	POs					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2		1	1		
CO2	2		1	1		
CO3	2		1	1		
CO4	2		1	1		
CO5	2		1	1		
Average	2		1	1		
1–Low, 2 –Medium, 3–High.						

(COMMON TO ALL BRANCHES)						
Programme & Branch	**M.E. VLSI DESIGN**	**CP**	**L**	**T**	**P**	**C**
		3	**3**	**0**	**0**	**3**

Course Objectives:

1	Analyze the significance of research and formulate well-defined research questions.
2	Apply appropriate research methods and critically evaluate research articles.
3	Create well-structured research papers and utilize research tools proficiently.
4	Produce effective technical reports and deliver impactful presentations.
5	Understand forms of intellectual property and analyze their implications on technological research and international cooperation.

UNIT–I	**CONCEPT OF RESEARCH**	**6+3**

Meaning and Significance of Research (L2)-Skills, Habits and Attitudes for Research (L1)-Time Management (L3) -Status of Research in India (L2)-Why, How, and What a Research is? (L2)-Types and Process of Research (L2)-Outcome of Research (L2)-Sources of Research Problem (L2)-Characteristics of a Good Research Problem (L2)-Errors in Selecting a Research Problem (L2)-Importance of Keywords (L1)-Literature Collection - Analysis (L2)-Citation Study - Gap Analysis (L2)-Problem Formulation Techniques (L2).

UNIT–II	**RESEARCH METHODS AND JOURNALS**	**6+3**

Interdisciplinary Research (L2)-Need for Experimental Investigations (L2)-Data Collection Methods (L3)-Appropriate Choice of Algorithms / Methodologies / Methods (L2)-Measurement and Result Analysis (L3)-Investigation of Solutions for Research Problem (L2)-Interpretation (L2)-Research Limitations (L2)-Journals in Science/Engineering (L2)-Indexing and Impact factor of Journals (L3)-Citations(L2)- h Index (L2)- i10 Index (L2)-Journal Policies (L4)How to Read a Published Paper (L2)-Ethical Issues Related to Publishing(L3)- Plagiarism and Self-Plagiarism (L2).

UNIT–III	**PAPER WRITING AND RESEARCH TOOLS**	**6+3**

Types of Research Papers (L2)- Original Article/Review Paper/Short Communication/Case Study(L2)-When and Where to Publish? (L2) - Journal Selection Methods (L2)-Layout of a Research Paper (L2)-Guidelines for Submitting the Research Paper (L2)-Review Process - Addressing Reviewer Comments (L3)-Use of tools / Techniques for Research (L3)-Hands-on Training related to Reference Management Software - EndNote (L3)- Introduction to Origin, SPSS,etc (L2)-Software for Detection of Plagiarism (L2)

UNIT–IV	**EFFECTIVE TECHNICAL THESIS WRITING/PRESENTATION**	**6+3**

How to Write a Report(L1)- - Language and Style (L1)-Format of Project Report (L1) - Use of Quotations (L2)-Method of Transcription Special Elements (L3)-Title Page - Abstract - Table of Contents - Headings and Sub-Headings (L2)-Footnotes - Tables and Figures - Appendix - Bibliography etc. (L3)-Different Reference Formats (L2)-Presentation using PPTs (L2).

UNIT–V	**NATURE OF INTELLECTUAL PROPERTY**	**6+3**

Patents(L1) - Designs(L2) - Trade and Copyright (L2)- Process of Patenting and Development (L2)-Technological research(L2)- innovation(L2)- - patenting(L2)-Development International Scenario (L2)-International Cooperation on Intellectual Property (L2)-Procedure for Grants of Patents (L2).

Total : 30+15=45 PERIODS

OPEN ENDED PROBLEMS / QUESTIONS

Course specific open ended problems will be solved during the classroom teaching. Such problems can be given as assignments and evaluated as internal assessment only and not for the end semester examination.

COURSE OUTCOMES: **Upon completion of this course the students will be able to:**	**BLOOM'S Taxonomy**

CO1	Illustrate the importance and objectives of research in contributing to knowledge and solving real-world problems.	L2 - Understand
CO2	Experiment with data collection techniques, choosing fitting approaches to ensure sound research framework and methodology.	L3 - Apply
CO3	Utilize research & analytic tools for enhancing the research publication	L2 - Understand
CO4	Apply knowledge to produce presentations and technical reports that effectively communicate research findings.	L3 - Apply
CO5	Explain types of intellectual property and comprehend patenting as essential for safeguarding innovation and creativity.	L2 - Understand

REFERENCE BOOKS:

1.	Cooper Donald R, Schindler Pamela S and Sharma JK, "Business Research Methods", Tata McGraw Hill Education, 11e (2012).
2.	DePoy, Elizabeth, and Laura N. Gitlin, "Introduction to Research-E-Book: Understanding and Applying Multiple Strategies", Elsevier Health Sciences, 2015.
3.	Walliman, Nicholas, "Research Methods: The basics", Routledge, 2017
4.	Bettig Ronald V., "Copyrighting culture: The political economy of intellectual property", Routledge, 2018.
5.	The Institute of Company Secretaries of India, Statutory body under an Act of parliament, "Professional Programme Intellectual Property Rights, Law and practice", September 2013.

VIDEO REFERENCES:

1.	https://www.youtube.com/watch?v=1vf8ZvADxfY&list=PLLhSIFfDZcUWRlgiXMkd1rNeLSz1You4O
2.	https://www.youtube.com/watch?v=eIUaS51U05M&list=PLIEVEMAFhG4_JmLtWGr6G0PRGB13xapyC

WEB REFERENCES:

1.	https://www.researchgate.net/
2.	https://www.wipo.int/about-ip/en/

ONLINE COURSES:

1.	https://onlinecourses.nptel.ac.in/noc23_ge36/preview
2.	https://onlinecourses.nptel.ac.in/noc22_hs59/preview

Mapping of COs with POs and PSOs

COs	POs						PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2
CO1	3	2	1			1		
CO2	3	3		2				
CO3	3			3	1			
CO4	3	3						
CO5	2	2		2		1		
Average	2.8	2.5	1	2.33	1	1		

1–Low, 2–Medium, 3–High.

ME23VL301	ANALOG IC DESIGN	Version: 1.0				
Programme &	M.E. VLSI DESIGN	CP	L	T	P	C

Branch		3	3	0	0	3

Course Objectives:

1	To design and analyze single stage amplifiers.
2	To characterize the high frequency and noise in amplifiers.
3	To characterize the parameters of single stage and multi stage op-amps.
4	To analyze stability and frequency compensation techniques in op-amps.
5	To design current sources and current sink circuits for band gap references.

UNIT–I	**SINGLE STAGE AMPLIFIERS**	**9**

Basic MOS physics and equivalent circuits and models (L2), CS, CG and Source Follower (L2), differential amplifier with active load (L2), Cascode and Folded Cascode configurations with active load (L3), design of Differential and Cascode Amplifiers – to meet specified SR (L3), noise, gain, BW, ICMR and power dissipation (L2), voltage swing (L2), high gain amplifier structures (L2).

UNIT–II	**HIGH FREQUENCY AND NOISE CHARACTERISTICS OF AMPLIFIERS**	**9**

Miller effect (L2), association of poles with nodes (L3), frequency response of CS, CG and Source Follower (L3), Cascode and Differential Amplifier stages (L2), statistical characteristics of noise (L3), noise in Single Stage amplifiers (L3), noise in Differential Amplifiers (L3).

UNIT– III	**FEEDBACK AND SINGLE STAGE OPERATIONAL AMPLIFIERS**	**9**

Properties and types of negative feedback circuits (L2), effect of loading in feedback networks (L3), operational amplifier performance parameters (L3), single stage Op Amps (L2), two-stage Op Amps (L2), input range limitations, gain boosting (L2), slew rate, power supply rejection, noise in Op Amps (L2)

UNIT – IV	**STABILITY AND FREQUENCY COMPENSATION OF TWO STAGE AMPLIFIER**	**9**

Analysis Of Two Stage Op Amp – Two Stage Op Amp Single Stage CMOS CS as Second Stage And Using Cascode Second Stage (L3), Multiple Systems, Phase Margin (L2), Frequency Compensation, And Compensation Of Two Stage Op Amps (L3), Slewing In Two Stage Op Amps (L3), Other Compensation Techniques (L2).

UNIT–V	**BANDGAP REFERENCES**	**9**

Current sinks and sources, current mirrors (L2), Wilson current source (L3), Widlar current source (L3), cascode current source, design of high swing cascode sink (L3), current amplifiers, supply independent biasing, temperature independent references (L3), PTAT and CTAT current generation (L2), constant-gm biasing (L3).

Total: 45 PERIODS

OPEN ENDED PROBLEMS / QUESTIONS

Course specific open ended problems will be solved during the classroom teaching. Such problems can be given as assignments and evaluated as internal assessment only and not for the end semester examination.

Course Outcomes: Upon completion of this course the students will be able to:		**BLOOM'S Taxonomy**
CO1	Design and analyze single stage amplifiers.	L3
CO2	Characterize the high frequency and noise in amplifiers.	L3
CO3	Characterize the parameters of single stage and multi stage op-amps.	L3
CO4	Analyze stability and frequency compensation techniques in op-amps.	L3
CO5	Design current sources and current sink circuits for band gap references.	L3

REFERENCE BOOKS:

1.	Behzad Razavi, "Design Of Analog Cmos Integrated Circuits", Tata Mcgraw Hill, 2001.
2.	Willey M.C. Sansen, "Analog Design Essentials", Springer, 2006.
3.	Grebene, "Bipolar And Mos Analog Integrated Circuit Design", John Wiley & Sons,Inc.,2003.
4.	Phillip E.Allen, Douglas R .Holberg, "Cmos Analog Circuit Design", Oxford University Press, 2nd Edition, 2002.
5.	Recorded Lecture Available at http://www.ee.iitm.ac.in/vlsi/courses/ee5320_2021/start
6.	Jacob Baker "CMOS: Circuit Design, Layout, And Simulation, Wiley IEEE Press, 3rd Edition, 2010.
VIDEO REFERENCES:	
1.	NPTEL :: Electronics & Communication Engineering - NOC:Analog IC Design
2.	https://youtube.com/playlist?list=PLbMVogVj5nJQB44z6h0XO2644Vbv7OM8_
WEB REFERENCES:	
1.	What is Analog Design? – Analog vs. Digital Design | Synopsys
2.	Education | Analog Devices
ONLINE COURSES:	
1.	Analog Ic Design - Course (nptel.ac.in)
2.	CMOS Analog Circuit Design | Udemy

Mapping of Cos with POs						
COs	**POs**					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	1	1	2	1		
CO2	1		2	1		
CO3	1		2	1	2	
CO4	1		2	1	2	
CO5	1		2	1	2	
Average	1	1	2	1	2	
1–Low, 2 –Medium, 3–High.						

ME23VL302	**DIGITAL CMOS VLSI DESIGN**	**Version: 1.0**				
Programme & Branch	**M.E. VLSI DESIGN**	**CP**	**L**	**T**	**P**	**C**
		3	**3**	**0**	**0**	**3**
Course Objectives:						

1	To analyze various characteristics of MOS transistors and CMOS inverter.
2	To design combinational circuits using different CMOS logic styles.
3	To characterize clocking strategies and clocking issues of sequential logic circuits.
4	To implement data path circuits such as adders, accumulators and multipliers.
5	To design memory units including ROM and SRAM.

UNIT–I	**MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER**	**9**
MOSFET characteristic under static and dynamic conditions (L2), MOSFET secondary effects (L3), Elmore constant (L3), CMOS inverter-static characteristic, dynamic characteristic (L2), power, energy, and energy delay parameters (L2), stick diagram and layout diagrams (L3).		
UNIT–II	**COMBINATIONAL LOGIC CIRCUITS**	**9**
Static CMOS design (L2), different styles of logic circuits (L2), logical effort of complex gates (L3), static and dynamic properties of complex gates (L3) interconnect delay, dynamic logic gates (L2).		
UNIT– III	**SEQUENTIAL LOGIC CIRCUITS**	**9**
Static latches and registers (L4), dynamic latches and registers (L4), timing issues (L3), pipelines, clocking strategies (L3), non bi-stable sequential circuits (L2)		
UNIT – IV	**ARITHMETIC BUILDING BLOCKS**	**9**
Data path circuits (L2), architectures for adders, accumulators (L2), multipliers, barrel shifters (L2), speed, power and area tradeoffs (L2).		
UNIT–V	**MEMORY ARCHITECTURES**	**9**
Memory architectures and Memory control circuits: Read-Only Memories (L2), ROM cells, Read Write Memories (RAM) (L3), dynamic memory design (L3), 6 Transistor SRAM cell (L3), sense amplifiers (L2).		
		Total: 45 PERIODS

OPEN ENDED PROBLEMS / QUESTIONS

Course specific open ended problems will be solved during the classroom teaching. Such problems can be given as assignments and evaluated as internal assessment only and not for the end semester examination.

Course Outcomes: Upon completion of this course the students will be able to:		**BLOOM'S Taxonomy**
CO1	Analyze the characteristics of MOS transistors and CMOS inverter.	L3 – Apply
CO2	Design combinational circuits using different CMOS logic styles.	L3 – Apply
CO3	Characterize clocking strategies and clocking issues of sequential logic circuits.	L4 – Analyse
CO4	Implement data path circuits such as adders, accumulators and multipliers.	L2 – Understand
CO5	Design memory units including ROM and SRAM.	L3 - Apply

REFERENCE BOOKS:

1.	N.Weste, K. Eshraghian, " Principles Of Cmos VLSI Design", Addision Wesley, 2nd Edition, 1993
2.	M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997
3.	Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis And Design", Mcgraw-Hill, 1998
4.	Jan Rabaey, Anantha Chandrakasan, B Nikolic, " Digital Integrated Circuits: A Design Perspective", Prentice Hall Of India, 2nd Edition, Feb 2003

VIDEO REFERENCES:

1.	CMOS Digital VLSI Design - YouTube

2.	EE141 - Spring 2012 - Digital Integrated Circuits - UC Berkeley - Jan M. Rabaey - YouTube
WEB REFERENCES:	
1.	CMOS VLSI Design and Circuit Simulation Tasks (cadence.com)
2.	Index of /~mcdermot/vlsi1/main/lectures (utexas.edu)
ONLINE COURSES:	
1.	CMOS Digital VLSI Design - Course (nptel.ac.in)
2.	Index of /classes/ece410/salem/files/s16/lectures (msu.edu)

Mapping of Cos with POs						
COs	**POs**					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	1		1	1		
CO2	1		2	1		
CO3	1		1	1		
CO4	1		2	1		
CO5	1		1	1		
Average	1		1.4	1		
1–Low, 2 –Medium, 3–High.						

ME23VL304	**ADVANCED DIGITAL SYSTEM DESIGN**	**Version: 1.0**				
Programme & Branch	**M.E. VLSI DESIGN**	**CP**	**L**	**T**	**P**	**C**
		3	**3**	**0**	**0**	**3**
Course Objectives:						
1	To design clocked synchronous sequential circuits.					

2	To analyze the asynchronous sequential circuits.
3	To apply the fault testing procedure for digital circuits.
4	To design the synchronous circuits using programmable devices.
5	To design and implement digital circuits using HDL programming.

UNIT–I	**SEQUENTIAL CIRCUIT DESIGN**	**9**

Analysis of Clocked Synchronous Sequential Circuits and Modeling- State Diagram (L4), State Table, State Table Assignment (L3) and Reduction-Design of Synchronous Sequential Circuits (L3), Design of Iterative Circuits-ASM Chart and Realization using ASM (L3).

UNIT–II	**ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN**	**9**

Analysis of Asynchronous Sequential Circuit – Flow Table Reduction (L4) -Races-State Assignment Transition Table and Problems in Transition Table (L4)- Design of Asynchronous Sequential Circuit - Static, Dynamic and Essential hazards (L3) – Mixed Operating Mode Asynchronous Circuits (L2) – Designing Vending Machine Controller (L2).

UNIT– III	**FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS**	**9**

Fault Table Method-Path Sensitization Method (L3) – Boolean Difference Method - D Algorithm (L3) – Tolerance Techniques – The Compact Algorithm (L3)– Fault in PLA – Test Generation (L3) - DFT Schemes – Built in Self Test (L3).

UNIT – IV	**SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES**	**9**

Programming Logic Device Families (L2)– Designing a Synchronous Sequential Circuit using PLA/PAL (L2) – Designing ROM with PLA (L2) – Realization of Finite State Machine using PLD (L2) – FPGA – Xilinx FPGA - Xilinx 4000 (L2).

UNIT–V	**SYSTEM DESIGN USING VERILOG**	**9**

Hardware Modeling with Verilog HDL (L2)– Logic System, Data Types And Operators For Modeling In Verilog HDL (L2) - Behavioral Descriptions In Verilog HDL (L2) – HDL Based Synthesis (L3)– Synthesis Of Finite State Machines– Structural Modeling (L3) – Compilation And Simulation Of Verilog Code (L3) – Test Bench - Realization Of Combinational And Sequential Circuits Using Verilog (L3) – Registers – Counters – Sequential Machine – Serial Adder – Multiplier- Divider – Design Of Simple Microprocessor (L3), Introduction To System Verilog (L2).

45 PERIODS

OPEN ENDED PROBLEMS / QUESTIONS

Course specific open ended problems will be solved during the classroom teaching. Such problems can be given as assignments and evaluated as internal assessment only and not for the end semester examination.

Course Outcomes: **Upon completion of this course the students will be able to:**		**BLOOM'S Taxonomy**
CO1	Design clocked synchronous sequential circuits.	L3 - Apply
CO2	Analyze the asynchronous sequential circuits.	L4 - Analyze
CO3	Apply the fault testing procedure for digital circuits.	L3 – Apply
CO4	Design the synchronous circuits using programmable devices.	L2–Understand
CO5	Design and implement digital circuits using HDL programming.	L4 - Apply

REFERENCE BOOKS:

1.	Charles H.Roth jr., "Fundamentals of Logic Design" Thomson Learning,2013.
2.	M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999
3.	M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.
4.	Nripendra N Biswas "Logic Design Theory" Prentice Hall of India,2001.
5.	Paragk.Lala "Fault Tolerant and Fault Testable Hardware Design" B S Publications,2002

6.	Paragk.Lala "Digital System Design Using PLD" B S Publications,2003
7.	Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003
VIDEO REFERENCES:	
1.	ECE 4305 – Advanced Digital Design Using System Verilog HDL – YouTube
2.	Digital System Design – YouTube
WEB REFERENCES:	
1.	Resources – Advanced Circuit Techniques Electrical Engineering and Computer Science – MIT Open Course Ware
2.	Advanced Circuit Techniques – Electrical Engineering and Computer Science – MIT Open Course Ware
ONLINE COURSES:	
1.	Digital System Design – Course (nptel.ac.in)
2.	Advanced Digital Design Course – VLSI Guru

Mapping of Cos with Pos						
Cos	**Pos**					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	1		1	1	1	
CO2	1		1	1	1	
CO3	1		1	1	1	
CO4	1		1	1	2	
CO5	1		1	1	1	
Average	1		1	1	1.2	
1–Low, 2 –Medium, 3–High.						

ME23VL304	**RFIC DESIGN**	**Version: 1.0**				
Programme & Branch	**M.E. VLSI DESIGN**	**CP**	**L**	**T**	**P**	**C**
		3	**3**	**0**	**0**	**3**
Course Objectives:						
1	To design impedance matching circuits for RF amplifiers.					

2	To design low noise amplifiers and RF power amplifiers.
3	To analyze the various parameters involved in RF mixers.
4	To design and analyze RF oscillators.
5	To design PLL and analyze frequency synthesizer

UNIT–I	**IMPEDANCE MATCHING IN AMPLIFIERS**	**9**

Definition of 'Q' (L2), Series Parallel Transformations of Lossy Circuits (L2) , Impedance Matching Using 'L', 'Pi' and T Networks (L2) , Integrated Inductors, Resistors, Capacitors, Tunable Inductors, Transformers (L2).

UNIT–II	**AMPLIFIER DESIGN**	**9**

Noise Characteristics of MOS Devices (L2), Design of CG LNA and Inductor Degenerated LNAs (L3). Principles of RF Power Amplifiers Design (L3)

UNIT– III	**ACTIVE AND PASSIVE MIXERS**	**9**

Qualitative Description of the Gilbert Mixer (L3) - Conversion Gain, and Distortion and Noise (L2), Analysis of Gilbert Mixer – Switching Mixer (L4) - Distortion in Unbalanced Switching Mixer (L3)-Conversion Gain in Unbalanced Switching Mixer (L3) - Noise in Unbalanced Switching Mixer (L3) - a Practical Unbalanced Switching Mixer (L4). Sampling Mixer - Conversion Gain in Single-Ended Sampling Mixer (L3) - Distortion in Single-Ended Sampling Mixer (L4) - Intrinsic Noise in Single-Ended Sampling Mixer (L3) - Extrinsic Noise in Single-Ended Sampling Mixer (L3)

UNIT – IV	**OSCILLATORS**	**9**

LC Oscillators, Voltage Controlled Oscillators (L3) , Ring Oscillators, Delay Cells (L3) , Tuning Range in Ring Oscillators (L3) , Tuning in LC Oscillators, Tuning Sensitivity (L2) , Phase Noise in Oscillators (L3) , Sources of Phase Noise (L2)

UNIT–V	**PLL AND FREQUENCY SYNTHESIZERS**	**9**

Phase Detector/Charge Pump (L2), Analog Phase Detectors, Digital Phase Detectors (L2) , Frequency Dividers, Loop Filter Design (L3) , Phase Locked Loops, Phase Noise in PLL, Loop Bandwidth (L3), Basic Integer-N Frequency Synthesizer (L3), Basic Fractional-N Frequency Synthesizer (L3)

45 PERIODS

OPEN ENDED PROBLEMS / QUESTIONS

Course specific open ended problems will be solved during the classroom teaching. Such problems can be given as assignments and evaluated as internal assessment only and not for the end semester examination.

Course Outcomes: **Upon completion of this course the students will be able to:**		**BLOOM'S Taxonomy**
CO1	Design impedance matching circuits for RF amplifiers.	L2 - Understand
CO2	Design low noise amplifiers and RF power amplifiers.	L3 – Apply
CO3	Analyze the various parameters involved in RF mixers.	L4 – Analyse
CO4	Design and analyze RF oscillators.	L3 - Apply
CO5	Design PLL and analyze frequency synthesizer	L3 - Apply

REFERENCE BOOKS:

1.	B.Razavi ,"RF Microelectronics" , Prentice-Hall ,1998
2.	Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002
3.	Behzad Razavi, "Design of Analog CMOS Integrated Circuits" Mcgraw-Hill, 1999
4.	Jia-Sheng Hong, "Microstrip Filters for RF/Microwave Applications", Wiley, 2001

5.	Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits', Cambridge University Press ,2003
VIDEO REFERENCES:	
1.	https://youtube.com/playlist?list=PLD60B441FD4FBF559&si=XJ7xRVOJSyRX4k8E
2.	https://youtu.be/2fVt_555TmI?si=30Y6UEG_lUQv0FSg
WEB REFERENCES:	
1.	https://www.ee.iitm.ac.in/~ani/2011/ee6240/lectures.html
2.	NPTEL :: Electronics & Communication Engineering - RF Integrated Circuits
ONLINE COURSES:	
1.	https://nptel.ac.in/courses/117102012

Mapping of COs with POs						
COs	**POs**					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2		2	2	2	
CO2	2		2	2	2	
CO3	1		2	2	2	
CO4	1		2	3	2	
CO5	2		2	2	2	
Average	1.6		2	2.2	2	
1–Low, 2 –Medium, 3–High.						

ME23PT801	**TECHNICAL SEMINAR / CASE STUDY PRESENTATION**	**Version : 1.0**				
(COMMON TO ALL BRANCHES)						
Programme & Branch	**M.E. VLSI DESIGN**	**CP**	**L**	**T**	**P**	**C**
		2	**0**	**0**	**2**	**1**
Course Objectives:						

1	To encourage the students to study advanced engineering developments
2	To prepare and present the technical and case study reports

Method of Evaluation:

The students need to identify an area of interest or topic in their programme of study or case study and prepare a 5-10 page report and a presentation. Based on the report and presentation, the course is evaluated for 100 marks. Minimum 50 marks is essential to pass. In case a student fails, he has to make such presentation in the subsequent semesters. The evaluation guidelines will be issued by the Head of the Department before the commencements of the course. The objectives are improving literature searching capabilities, comprehension and ability to write reports and to make presentations. It is assessed in Internal Assessment mode only and no End Semester Examination.

Total : 30 PERIODS

Course Outcomes: At the end of this course, the students will demonstrate the ability to		**BLOOM'S Taxonomy**
CO1	Perform the review and present technological developments in their field	L3 - Apply
CO2	Interpret the case study report and make a decision	L3 - Apply

Mapping of COs with POs						
CO	**PO**					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
1		3				
2		3				
Avg		3				
1–Low, 2 –Medium, 3–High.						

ME23VL305	FPGA Laboratory	Version: 1.0				
Programme & Branch	M.E. VLSI DESIGN	CP	L	T	P	C
		4	0	0	4	2

Course Objectives:

1.	To study the basics of HDL programming and simulator tools.
2.	To design and verify ALU and Instruction stack.
3.	To generate test program for combinational and sequential circuit.
4.	To develop a test bench using object oriented structure.
5.	To develop and verify test environments with various constraints.

LIST OF EXPERIMENTS

1.	Introduction to Verilog and System Verilog
2.	Running simulator and debug tools
3.	Experiment with 2 state and 4 state data types
4.	Experiment with blocking and non-blocking assignments
5.	Model and verify simple ALU
6.	Model and verify an Instruction stack
7.	Use an interface between testbench and DUT
8.	Developing a test program
9.	Create a simple and advanced OO testbench
10.	Create a scoreboard using dynamic array
11.	Use mailboxes for verification
12.	Generate constrained random test values
13.	Using coverage with constrained random tests

TOTAL: 60PERIODS

COURSE OUTCOMES		**BLOOM'S Taxonomy**
CO 1	Comprehend the basics of HDL programming and simulator tools.	L2 – Understand
CO 2	Design and verify ALU and Instruction stack.	L3 – Apply
CO 3	Generate test program for combinational and sequential circuit.	L3 – Apply
CO 4	Develop a test bench using object oriented structure.	L3 – Apply
CO 5	Develop and verify test environments with various constraints.	L3 – Apply

Mapping of COs with POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1			3	2	
CO2	1			3	2	
CO3	1			3	2	
CO4	1			3	2	
CO5	1			3	2	
Average						

1–Low, 2 –Medium, 3–High.

ME23VL306	ANALOG IC DESIGN LABORATORY	Version: 1.0				
Programme & Branch	M.E. VLSI DESIGN	CP	L	T	P	C
		4	0	0	4	2

Course Objectives:

1	To design and analyse the various parameters of digital CMOS circuits for a given specification.
2	To build and verify the SPICE models of oscillator circuits.
3	To design and characterize single stage amplifier circuits for a given specification.
4	To design and characterize instrumentation amplifier circuit.
5	To design and extract circuit parameters using layout editor tool.

LIST OF EXPERIMENTS

1	Extraction of process parameters of CMOS process transistors a. Plot ID vs. VGS at different drain voltages for NMOS, PMOS. b. Plot ID vs. VGS at particular drain voltage for NMOS, PMOS and determine Vt. c. Plot log ID vs. VGS at particular gate voltage for NMOS, PMOS and determine IOFF and sub threshold slope. d. Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor. e. Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS of appropriate voltage To extract Vth use the following procedure. i. Plot gm vs VGS using SPICE and obtain peak gm point. ii. Plot y=ID/(gm) as a function of VGS using SPICE. iii. Use SPICE to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth. f. Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency. Tabulate result according to technologies and comment on it.
2	CMOS inverter design and performance analysis a. i. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter. ii. Plot VTC for CMOS inverter with varying VDD. iii. Plot VTC for CMOS inverter with varying device ratio. b. Perform transient analysis of CMOS inverter with no load and with load and determine propagation delay tpHL, tpLH, 20%-to-80% rise time tr and 80%-to-20% fall time tf. c. Perform AC analysis of CMOS inverter with fanout 0 and fanout 1.
3	Use spice to build a three stage and five stage ring oscillator circuit and compare its frequencies. Use FFT and verify the amplitude and frequency components in the spectrum
4	Single stage amplifier design and performance analysis a. Plot small signal voltage gain of the minimum-size inverter in the technology chosen as a function of input DC voltage. Determine the small signal voltage gain at the switching point using spice and compare the values for two different process transistors. b. Consider a simple CS amplifier with active load, with NMOS transistor as driver and PMOS transistor as load. i. Establish a test bench to achieve VDSQ=VDD/2. ii. Calculate input bias voltage for a given bias current. iii. Use spice and obtain the bias current. Compare with the theoretical value iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier v. using small signal analysis in spice, considering load capacitance. vi. Plot step response of the amplifier with a specific input pulse amplitude. vii. Derive time constant of the output and compare it with the time constant viii. Resulted from -3dB Band Width. ix. Use spice to determine input voltage range of the amplifier

5	Three OPAMP Instrumentation Amplifier (INA). a. Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage. i. Draw the schematic of op-amp macro model. ii. Draw the schematic of INA. iii. Obtain parameters of the op-amp macro model such that meets a given specification for: i. low-frequency voltage gain, ii. unity gain BW (fu) iii. input capacitance iv. output resistance v. CMRR b. Draw schematic diagram of CMRR simulation setup. c. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP). d. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. e. Explain how CMRR of OPAMP changes with resistor mismatches. f. Repeat (iii) to (vi) by considering CMRR of all OPAMPs with low frequency gain setting.
6	Use Layout editor. a. Draw layout of a minimum size inverter using transistors from CMOS process library. Use Metal 1 as interconnect line between inverters. b. Run DRC, LVS and RC extraction. Make sure there is no DRC error. c. Extract the netlist. Use extracted netlist and obtain tPHLtPLH for the inverter using Spice. d. Use a specific interconnect length and connect and connect three inverters in a chain. e. Extract the new netlist and obtain tPHL and tPLH of the middle inverter. f. Compare new values of delay times with corresponding values obtained in part 'c'.
7	Design a differential amplifier with resistive load using transistors from CMOS process library that meets a given specification for the following parameter a. low-frequency voltage gain, b. unity gain BW (fu), c. Power dissipation i. Perform DC analysis and determine input common mode range and compare with the theoretical values. ii. Perform time domain simulation and verify low frequency gain. iii. Perform AC analysis and verify.
	TOTAL: 60PERIODS

COURSE OUTCOMES		**BLOOM'S Taxonomy**
CO 1	Design and analyse the various parameters of digital CMOS circuits for a given specification.	L3 – Apply
CO 2	Build and verify the SPICE models of oscillator circuits.	L3 – Apply
CO 3	Design and characterize single stage amplifier circuits for a given specification.	L3 – Apply
CO 4	Design and characterize instrumentation amplifier circuit.	L3 – Apply
CO 5	Design and extract circuit parameters using layout editor tool.	L3 – Apply

Mapping of COs with POs						
COs	**POs**					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	1			3	2	
CO2	1			3	2	
CO3	1			3	2	
CO4	1			3	2	
CO5	1			3	2	
Average						
1–Low, 2 –Medium, 3–High.						

II SEMESTER

Programme & Branch	M.E. VLSI DESIGN	CP	L	T	P	C
		3	3	0	0	3

Course Objectives:

1	To provide the students complete understanding on UVM testing
2	To become proficient at UVM verification,
3	To provide an experience on self-checking UVM test benches

UNIT–I	INTRODUCTION	9

Overview- The Typical UVM Testbench Architecture (L2)- The UVM Class Library (L2) -Transaction-Level Modeling (TLM) (L2) -Overview- TLM, TLM-1, and TLM-2.0 (L2) -TLM-1 Implementation (L2) - TLM-2.0 Implementation (L2)

UNIT–II	DEVELOPING REUSABLE VERIFICATION COMPONENTS	9

Modeling Data Items for Generation (L3)- Transaction-Level Components - Creating the Driver - Creating the Sequencer (L3) - Connecting the Driver and Sequencer -Creating the Monitor (L3) - Instantiating Components- Creating the Agent (L3) - Creating the Environment -Enabling Scenario Creation (L3) - Managing of Test-Implementing Checks and Coverage (L3)

UNIT– III	UVM USING VERIFICATION COMPONENTS	9

Creating a Top-Level Environment- Instantiating Verification Components (L3) - Creating Test Classes - Verification Component Configuration (L3) - Creating and Selecting a User-Defined Test (L3) - Creating Meaningful Tests- Virtual Sequences (L3) - Checking for DUT Correctness- Scoreboards (L3) - Implementing a Coverage Model (L3)

UNIT – IV	UVM USING THE REGISTER LAYER CLASSES	9

Using The Register Layer Classes - Back-Door Access -Special Registers -Integrating a Register- Model in a Verification Environment- Integrating a Register Model- Randomizing Field Values- Pre-Defined Sequences

UNIT–V	ASSIGNMENT IN TESTBENCHES	9

Assignment, APB: Protocol (L2), Test bench Architecture (L2) , Driver and Sequencer V , Monitor, Agent and Environment (L2); Creating Sequences, Building Test (L2) , Design and Testing of Top Module (L2)

45 PERIODS

	OPEN ENDED PROBLEMS / QUESTIONS	

Course specific open ended problems will be solved during the classroom teaching. Such problems can be given as assignments and evaluated as internal assessment only and not for the end semester examination

Course Outcomes: Upon completion of this course the students will be able to:		BLOOM'S Taxonomy
CO1	Understand the basic concepts of two methodologies UVM	L2 – Understand
CO2	Build actual verification components	L3 – Apply
CO3	Generate the register layer classes.	L3 – Apply
CO4	Code test benches using UVM.	L3 – Apply
CO5	Understand advanced peripheral bus testbenches	L2 – Understand

REFERENCE BOOKS:

1.	The UVM Primer, An Introduction to the Universal Verification Methodology, Ray Salemi, 2013.
2.	System Verilog for Verification: A Guide to Learning the Testbench Language Features, Chris Spear, Greg Tumbush, 3rd edition, 2012.
3.	https://www.udemy.com/learn-ovm-UVM/ 2.
4.	http://www.testbench.in/ut_00_index.html 3.
5.	http://www.testbench.in/ot_00_index.html
6.	https://www.accellera.org/images/downloads/standards/UVM/UVM_users_guide_1.2.pdf
VIDEO REFERENCES:	
1.	https://youtu.be/2026Ei1wGTU
2.	https://youtu.be/8F5nLB5zL-0
WEB REFERENCES:	
1.	Guide - Developing Reusable Verification Components (chipverify.com)
2.	RTL Design - APB Protocol | QuickSilicon - YouTube
ONLINE COURSES:	
1.	UVM for Verification Part 1 : Fundamentals | Udemy
2.	UVM for Verification Part 2 : Projects | Udemy

Mapping of COs with POs						
COs	**POs**					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	1		1	1	2	
CO2	1		1	1	2	
CO3	1		1	1	2	
CO4	1		1	1	2	1
CO5	1		1	1	2	1
Average	1		1	1	2	1

Programme & Branch	M.E. VLSI DESIGN	CP	L	T	P	C
		3	3	0	0	3

Instructions if any

Course Objectives:

1	Identify sources of power in an IC.
2	Identify the power reduction techniques based on technology independent and technology dependent methods
3	Identify suitable techniques to reduce the power dissipation
4	Estimate power dissipation of various MOS logic circuits
5	Develop algorithms for low power dissipation

UNIT–I	POWER DISSIPATION IN CMOS	9

Hierarchy of Limits of Power (L2)– Sources of Power Consumption (L2) – Physics of Power Dissipation in CMOS FET Devices (L2) – Basic Principle of Low Power Design (L2).

UNIT–II	POWER OPTIMIZATION	9

Logic Level Power Optimization (L2) – Circuit Level Low Power Design (L2) – Gate Level Low Power Design (L2) –Architecture Level Low Power Design (L2) – VLSI Subsystem Design of Adders, Multipliers (L3), PLL, Low Power Design (L2).

UNIT– III	DESIGN OF LOW POWER CMOS CIRCUITS	9

Computer Arithmetic Techniques for Low Power System (L2) – Reducing Power Consumption in Combinational Logic, Sequential Logic, Memories (L3) – Low Power Clock – Advanced Techniques (L3) – Special Techniques (L3), Adiabatic Techniques – Physical Design, Floor Planning, Placement and Routing (L3).

UNIT – IV	POWER ESTIMATION	9

Power Estimation Techniques (L3), Circuit Level, Gate Level, Architecture Level, Behavioral Level, – Logic Power Estimation (L4) – Simulation Power Analysis (L3) –Probabilistic Power Analysis (L4)

UNIT–V	SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER CMOS CIRCUITS	9

Synthesis for Low Power – Behavioral Level Transform (L3) –Algorithms for Low Power (L3) – Software Design for Low Power (L3).

45 PERIODS

OPEN ENDED PROBLEMS / QUESTIONS

Course specific open ended problems will be solved during the classroom teaching. Such problems can be given as assignments and evaluated as internal assessment only and not for the end semester examination

Course Outcomes: **Upon completion of this course the students will be able to:**		**BLOOM'S Taxonomy**
CO1	Able to find the power dissipation of MOS circuits	L2 – Understand
CO2	Design and analyze various MOS logic circuits	L3 – Apply
CO3	Apply low power techniques for low power dissipation	L3 – Apply
CO4	Able to estimate the power dissipation of ICs	L4 – Analyze
CO5	Able to develop algorithms to reduce power dissipation by software tools.	L3 - Apply

REFERENCE BOOKS:	
1.	Kaushik Roy and S.C.Prasad, "Low Power CMOS VLSI Circuit Design", Wiley, 2000
2.	J.B.Kulo and J.H Lou, "Low Voltage CMOS VLSI Circuits", Wiley 1999.
3.	James B.Kulo, Shih-Chia Lin, "Low Voltage SOI CMOS VLSI Devices and Circuits", John Wiley and Sons, Inc. 2001
4.	J.Rabaey, "Low Power Design Essentials (Integrated Circuits and Systems)", Springer, 2009
VIDEO REFERENCES:	
1.	https://youtube.com/playlist?list=PLbMVogVj5nJTDr6KqQXNcxCvooSMnBuXj
2.	https://youtube.com/playlist?list=PLB3F0FC99B5D89571
WEB REFERENCES:	
1.	NPTEL :: Computer Science and Engineering - Low Power VLSI Circuits & Systems
2.	Low Power Design Methodology | IntechOpen
ONLINE COURSES:	
1.	VLSI System Design & SubSystems of Digital Circuits Course | Udemy

Mapping of COs with POs						
COs	**POs**					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2		2	3	2	
CO2	2		2	2	2	
CO3	1		2	2	2	
CO4	1		2	3	2	
CO5	2		2	2	3	
Average	1.6		2	2.4	2.2	

Programme & Branch	M.E. VLSI DESIGN	CP	L	T	P	C
		3	3	0	0	3

Instructions if any

Course Objectives:

1	To introduce the VLSI testing.
2	To introduce logic and fault simulation and testability measures
3	To study the test generation for combinational and sequential circuits
4	To study the design for testability.
5	To study the fault diagnosis

UNIT–I	INTRODUCTION TO TESTING	9

Introduction – VLSI Testing Process and Test Equipment (L2)– Challenges in VLSI Testing - Test Economics and Product Quality (L2)– Fault Modeling – Relationship Among Fault Models (L2).

UNIT–II	LOGIC & FAULT SIMULATION & TESTABILITY MEASURES	9

Simulation for Design Verification and Test Evaluation (L3) – Modeling Circuits for Simulation (L3) – Algorithms for True Value and Fault Simulation (L3) – Scoap Controllability and Observability (L3)

UNIT– III	TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS	9

Algorithms and Representations (L3) – Redundancy Identification – Combinational ATPG Algorithms (L3) – Sequential ATPG Algorithms (L3) – Simulation Based ATPG (L3) – Genetic Algorithm Based ATPG (L3)

UNIT – IV	DESIGN FOR TESTABILITY	9

Design for Testability Basics (L2) – Testability Analysis - Scan Cell Designs (L2) – Scan Architecture (L2) – Built-in Self-Test (L2) – Random Logic Bist (L2) – DFT for Other Test Objectives (L2).

UNIT–V	FAULT DIAGNOSIS	9

Introduction and Basic Definitions – Fault Models for Diagnosis (L3) – Generation of Vectors for Diagnosis (L3) – Combinational Logic Diagnosis (L3) - Scan Chain Diagnosis – Logic BIST Diagnosis (L3).

45 PERIODS

OPEN ENDED PROBLEMS / QUESTIONS

Course specific open ended problems will be solved during the classroom teaching. Such problems can be given as assignments and evaluated as internal assessment only and not for the end semester examination

Course Out comes: Upon completion of this course the students will be able to:		**BLOOM'S Taxonomy**
CO1	Understand VLSI Testing Process	L2 – Understand
CO2	Develop Logic Simulation and Fault Simulation	L3 – Apply
CO3	Develop Test for Combinational and Sequential Circuits	L3 – Apply
CO4	Understand the Design for Testability	L2 – Understand
CO5	Perform Fault Diagnosis.	L3 – Apply

REFERENCE BOOKS:

1.	Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, "VLSI Test Principles and Architectures", Elsevier, 2017
2.	Michael L. Bushnell and Vishwani D. Agrawal, "Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits" , Kluwer Academic Publishers, 2017.
3.	Niraj K. Jha and Sandeep Gupta, "Testing of Digital Systems", Cambridge University Press, 2017.
VIDEO REFERENCES:	
1.	https://youtube.com/playlist?list=PLbMVogVj5nJTClnafWQ9FK2nt3cGG8kCF&si=KsCdiDSXxro72ARc
2.	https://youtube.com/playlist?list=PLx98Qgh5zPjh6oWI73QfQHZAmAiyt8Wkf&si=W7cJqNXn8EuHtDPo
WEB REFERENCES:	
1.	https://archive.nptel.ac.in/content/storage2/courses/106103116/handout/mod7.pdf
2.	https://archive.nptel.ac.in/courses/117/105/117105137/
ONLINE COURSES:	
1.	https://nptel.ac.in/courses/117105137
2.	https://onlinecourses.nptel.ac.in/noc20_ee76/preview

Mapping of COs with POs

COs	POs					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2		2	3	3	1
CO2	2		2	2	3	1
CO3	1		2	2	3	1
CO4	1		2	3	2	1
CO5	2		2	2	1	1
Average	1.6		2	2.4	2.4	1

Branch		4	0	0	4	2

Course Objectives:

1.	To help the engineers to design the system with verilog and system Verilog
2.	Complete understanding of Verilog Hardware Description Language
3.	To practice for writing synthesizable RTL models that work correctly in both simulation and synthesis.

LIST OF EXPERIMENTS

1.	Simulate a simple UVM testbench and DUT
2.	Examining the UVM testbench
3.	Design and simulate sequence items and sequence
4.	Design and simulate a UVM driver and sequencer
5.	Design and simulating UVM monitor and agent
6.	Design, simulate and examine coverage
7.	Design and simulate a UVM scoreboard and environment, and verifying the outputs of a (faulty) DUT
8.	Design and simulate a test that runs multiple sequence
9.	Design and simulate a configurable UVM test environment

TOTAL: 60PERIODS

COURSE OUTCOMES		**BLOOM'S Taxonomy**
CO 1	Understand the features and capabilities of the UVM class library for system Verilog	L3 – Apply
CO 2	Combine multiple UVCs into a complete verification environment	L3 – Apply
CO 3	Create and configure reusable, scalable, and robust UVM verification components (UVCs).	L3 – Apply
CO 4	Create a UVM testbench structure using the UVM library base classes and the UVM factory	L3 – Apply
CO 5	Develop a register model for your DUT and use the model for initialization and accessing DUT registers	L3 – Apply

Mapping of COs with POs

COs	**POs**					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	1			3	2	
CO2	1			3	2	
CO3	1			3	2	
CO4	1			3	2	
CO5	1			3	2	
Average	1			3	2	
1–Low, 2 –Medium, 3–High.						

AUDIT COURSES

ME23AC701	ENGLISHFORRESEARCHPAPERWRITING	Version: 1.0
(COMMON TO ALL BRANCHES)		

Programme & Branch	M.E- VLSI DESIGN	CP	L	T	P	C
		2	2	0	0	0

Course Objectives:

1	To teach how to improve writing skills and level of readability
2	To tell about what to write in each section
3	To summarize the skills needed when writing a title
4	To infer the skills needed when writing the conclusion
5	To ensure the quality of paper at very first-time submission

UNIT–I	INTRODUCTIONTORESEARCH PAPERWRITING	6

Planning and Preparation (L2), Word Order (L1), Breaking up long sentences (L2), Structuring Paragraphs and Sentences (L1), Being Concise and Removing Redundancy (L1),Avoiding Ambiguity and Vagueness (L2).

UNIT–II	PRESENTATION SKILLS	6

Clarifying Who Did What (L2), Highlighting Your Findings (L1), Hedging and Criticizing (L1), Paraphrasing and Plagiarism (L1), Sections of a Paper (L1), Abstracts, Introduction (L1).

UNIT–III	TITLEWRITINGSKILLS	6

Key skills are needed when writing a Title (L1), key skills are needed when writing an Abstract (L1), key skills are needed when writing an Introduction (L1), skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check (L1).

UNIT–IV	RESULTWRITINGSKILLS	6

Skills are needed when writing the Methods (L1), skills needed when writing the Results (L2), skills are needed when writing the Discussion (L2), skills are needed when writing the Conclusions (L2).

UNIT–V	VERIFICATIONSKILLS	6

Useful phrases (L1), checking Plagiarism (L1), how to ensure paper is as good as it could possibly be the first- time submission (L1).

TOTAL: 45 PERIODS

OPEN ENDED PROBLEMS /QUESTIONS		
Course specific open ended problems will be solved during the classroom teaching. Such problems can be given as assignments and evaluated as internal assessment only and not for the end semester examination		
Course Outcomes: **Upon completion of this course the students will be able to:**		**BLOOMS Taxonomy**
CO1	Understand that how to improve your writing skills and level of readability	L2 – Understand
CO2	Learn about what to write in each section	L1 – Remember
CO3	Understand the skills needed when writing a Title	L2 – Understand
CO4	Understand the skills needed when writing the Conclusion	L2 – Understand
CO5	Ensure the good quality of paper at very first-time submission	L2 – Understand
TEXT BOOKS:		
1.	Adrian Wall work, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.	
2.	Day R How to Write and Publish a Scientific Paper, Cambridge University Press 2006.	
REFERENCE BOOKS:		
1.	Goldbort R Writing for Science, Yale University Press (available on Google Books)2006.	
2.	HighmanN, Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book 1998.	

ME23AC702	DISASTERMANAGEMENT	Version: 1.0
(COMMON TO ALL BRANCHES)		

Programme& Branch	M.E- VLSI DESIGN	CP	L	T	P	C
		2	2	0	0	0

Course Objectives:

1	Summarize basics of disaster
2	Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
3	Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
4	Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
5	Develop the strengths and weaknesses of disaster management approaches

UNIT–I	INTRODUCTION	6

Disaster: Definition (L1), Factors and Significance(L1); Difference between Hazard And Disaster(L2); Natural and Manmade Disasters: Difference, Nature, Types and Magnitude(L1).

UNIT–II	REPERCUSSIONSOFDISASTERSANDHAZARDS	6

Economic Damage (L1), Loss of Human and Animal Life (L1), Destruction Of Ecosystem (L1). Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches (L1), Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts (L1).

UNIT–III	DISASTERPRONEAREASININDIA	6

Study of Seismic Zones (L1); Areas Prone To Floods and Droughts (L1), Landslides And Avalanches (L1); Areas Prone To Cyclonic and Coastal Hazards with Special Reference To Tsunami (L1); Post-Disaster Diseases and Epidemics (L1)

UNIT–IV	DISASTERPREPAREDNESSANDMANAGEMENT	6

Preparedness: Monitoring Of Phenomena Triggering a Disaster or Hazard (L2); Evaluation of Risk: Application of Remote Sensing (L1), Data from Meteorological And Other Agencies (L1), Media Reports: Governmental and Community Preparedness (L1).

UNIT–V	RISKASSESSMENT	6

Disaster Risk: Concept and Elements (L1), Disaster Risk Reduction (L1), Global and National Disaster Risk Situation (L1).Techniques of Risk Assessment (L1),Global Co-Operationin Risk Assessment andWarning (L1), People's Participation in Risk Assessment. Strategies for Survival (L1)

TOTAL: 45 PERIODS

OPEN ENDED PROBLEMS /QUESTIONS		
Course specific open ended problems will be solved during the classroom teaching. Such problems can be given as assignments and evaluated as internal assessment only and not for the end semester examination		
Course Outcomes: **Upon completion of this course the students will be able to:**		**BLOOMS Taxonomy**
CO1	Summarize basics of disaster	L1 – Remember
CO2	Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.	L2 – Understand
CO3	Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives	L2 – Understand
CO4	Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.	L2 – Understand
CO5	Develop the strengths and weaknesses of disaster management approaches	L2 – Understand
TEXTBOOKS:		
1.	GoelS.L., Disaster Administration And Management Text And Case Studies", Deep& Deep Publication Pvt. Ltd., New Delhi, 2009.	
2.	Nishitha Rai, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company, 2007.	
REFERENCE BOOKS:		
1.	Sahni, Pradeep Et.Al.,"Disaster Mitigation Experiences And Reflections", Prentice Hall of India, New Delhi,2001.	

ME23AC703	CONSTITUTION OF INDIA	Version: 1.0
(COMMON TO ALL BRANCHES)		

Programme& Branch	M.E- VLSI DESIGN	CP	L	T	P	C
		2	2	0	0	0

Course Objectives:

1	To understand the premises in forming the twin themes of liberty and freedom from a civil rights perspective.
2	To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional
3	To role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
4	To address the role of socialism in India after the commencement of the Bolshevik Revolution 1917 And its impact on the initial drafting of the Indian Constitution

UNIT–I	HISTORYOFMAKINGOFTHEINDIANCONSTITUTION	6
History(L1), Drafting Committee(L1), (Composition & Working)		
UNIT–II	**PHILOSOPHY OF THE INDIAN CONSTITUTION**	**6**
Preamble (L1), Salient Features(L1).		
UNIT–III	**CONTOURSOFCONSTITUTIONALRIGHTSANDDUTIES**	**6**
Fundamental Rights (L1), Right to Equality (L1), Right to Freedom (L1), Right against Exploitation (L1), Right to Freedom of Religion (L1), Cultural and Educational Rights (L1), Right to Constitutional Remedies (L1), Directive Principles of State Policy (L1), Fundamental Duties (L1).		
UNIT–IV	**ORGANS OF GOVERNANCE**	**6**
Parliament (L1), Composition (L1), Qualifications and Disqualifications (L1), Powers and Functions (L1), Executive (L1), President (L1), Governor (L1), Council of Ministers (L1), Judiciary, Appointment and Transfer of Judges (L1), Qualifications, Powers and Functions (L1).		
UNIT–V	**LOCALADMINISTRATION**	**6**
District's Administration head: Role and Importance (L1), Municipalities: Introduction, Mayor and role of Elected Representative, CEO, Municipal Corporation (L1). Pachayati raj: Introduction (L1), PRI: Zila Panchayat (L1). Elected officials and their roles (L1), CEO Zila Pachayat: Position and role (L1). Block level: Organizational Hierarchy (Different departments) (L1), Village level:Role of Elected and Appointed officials (L1), Importance of grass root democracy (L1).		
UNIT–VI	**ELECTIONCOMMISSION**	**6**
Election Commission: Role and Functioning (L1). Chief Election Commissioner and Election Commissioners (L1) - Institute and Bodies for the welfare of SC/ST/OBC and women (L1).		

Total:- 45 PERIODS

OPEN ENDED PROBLEMS /QUESTIONS

Course specific open ended problems will be solved during the classroom teaching. Such problems can be given as assignments and evaluated as internal assessment only and not for the end semester examination

Course Outcomes: **Upon completion of this course the students will be able to:**		**BLOOMS Taxonomy**
CO1	Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.	L2 – Understand
CO2	Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.	L2 – Understand

CO3	Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.	L2 – Understand
CO4	Discuss the passage of the Hindu Code Bill of 1956.	L2 – Understand
TEXTBOOKS:		
1.	The Constitution of India,1950(Bare Act),Government Publication	
2.	Dr.S.N.Busi, Dr.B.R.Ambedkar framing of Indian Constitution, 1st Edition, 2015.	
REFERENCE BOOKS:		
1.	M.P.Jain, Indian Constitution Law,7th Edn.,LexisNexis,2014.	
2.	D.D.Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.	

ME23AC704	நற்றமிழ் இலக்கியம்	Version: 1.0
(COMMON TO ALL BRANCHES)		

Programme & Branch	M.E- VLSI DESIGN	CP	L	T	P	C
		2	2	0	0	0

Course Objectives:

1	சங்க இலக்கியம் பற்றி மாணவர்களுக்கு எடுத்துரைத்தல்
2	நீதிநூல்கள் வாயிலாக அறக்கருத்துகளை எடுத்து கூறுதல்.
3	சிலப்பதிகாரம் மணிமேகலை காப்பியங்களை எடுத்துரைத்தல்.
4	இலக்கியங்களில் காணப்படும் அருள் நெறிக் கதைகளைப்பற்றி விளக்குதல்.
5	தற்காலத் தமிழ் இலக்கியங்களை மாணவர்களுக்கு தெரியப்படுத்துதல்.

UNIT–I சங்க இலக்கியம் **6**

1. தமிழின் துவக்க நூல் தொல்காப்பியம் - எழுத்து, சொல், பொருள் (L1)
2. அகநானூறு (82) - இயற்கை இன்னிசை அரங்கம் (L1)
3. குறிஞ்சிப் பாட்டின் மலர்க்காட்சி (L1)
4. புறநானூறு (95, 195) – போரை நிறுத்திய ஔவையார் (L1)

UNIT–II அறநெறித்தமிழ் **6**

1. அறநெறி வகுத்த திருவள்ளுவர் - அறம் வலியுறுத்தல், அன்புடைமை, ஒப்புறவு அறிதல், ஈகை, புகழ் (L2)
2. பிற அறநூல்கள் - இலக்கிய மருந்து - ஏலாதி, சிறுபஞ்சமூலம், திரிகடுகம், ஆசாரக்கோவை (தூய்மையை வலியுறுத்தும் நூல்) (L2)

UNIT–III இரட்டைக்காப்பியங்கள் **6**

1. கண்ணகியின் புரட்சி- சிலப்பதிகார வழக்குரை காதை (L1)
2. சமூக சேலை இலக்கியம் மணிமேகலை - சிறைக்கோட்டம் அறக்கோட்டமாகிய காதை (L1)

UNIT–IV அருள்நெறித்தமிழ் **6**

1. சிறுபாணாற்றுப்படை - பாரி முல்லைக்கு தேர் கொடுத்தது, பேகன் மயிலுக்குப் போர்வை கொடுத்தது, அதியமான் ஔவைக்கு நெல்லிக்கனி கொடுத்தது, அரசர் பண்புகள். (L2)
2. நற்றிணை - அன்னைக்குரிய புன்னை சிறப்பு (L2)
3. திருமந்திரம் (617,618) இயமம் நியமம் விதிகள் (L2)
4. தர்மசாலையை நிறுவிய வள்ளலார் (L2)
5. புறநானூறு - சிறுவனே வள்ளலானான் (L2)
6. அகநானூறு (4) - வண்டு (L2)
7. நற்றிணை (11) - நண்டு (L2)
8. கலித்தொகை (11) - யானை, புறா (L2)
9. ஐந்திணை ஐம்பது (27) - மான் (L2) ஆகியவை பற்றிய செய்திகள் (L2)

UNIT–V நவீன தமிழ் இலக்கியம் **6**

1. உரைநடைத்தமிழ் (L1)
   - தமிழின் முதல் புதினம் (L1)
   - தமிழின் முதல் சிறுகதை (L1)
   - கட்டுரை இலக்கியம் (L1)
   - பயண இலக்கியம் (L1)
   - நாடகம் (L1)
2. நாட்டு விடுதலை போராட்டமும் தமிழ் இலக்கியமும் (L1)
3. சமுதாய விடுதலையும் தமிழ் இலக்கியமும் (L1)
4. பெண் விடுதலையும் விளிம்பு நிலையினரின் மேம்பாட்டில் தமிழ் இலக்கியமும் (L1)
5. அறிவியல் தமிழ் (L1)
6. இணையத்தில் தமிழ் (L1)

7. சுற்றுச்சூழல் மேம்பாட்டில் தமிழ் இலக்கியம் (L1)
Total: 30 PERIODS

OPEN ENDED PROBLEMS /QUESTIONS		
Course Outcomes: **Upon completion of this course the students will be able to:**		**BLOOMS Taxonomy**
CO1	சங்க இலக்கியம் மாணவர்கள் முழுமையாக அறிந்து பயன்பெறுதல்.	L1 - நினைவில் கொள்ளுதல்
CO2	அறநெறி இலக்கியம் வாயிலாக வாழ்வியலுக்குத் தேவையான தூய்மைப் பணிகளை மேற்கொள்ளுதல்.	L2 - புரிந்து கொள்ளுதல்
CO3	சிலப்பதிகாரம், மணிமேகலை காப்பியங்களில் உள்ள நீதிக்கருத்துகளை மாணவர்கள் தெரிந்துகொள்ளுதல்.	L1 - நினைவில் கொள்ளுதல்
CO4	இலக்கியங்களில் காணப்படும் அருள்நெறிக் கதைகளைப் பற்றி விளக்குதல்.	L2 - புரிந்து கொள்ளுதல்
CO5	தற்காலத் தமிழ் இலக்கியங்களை மாணவர்கள் தெரிந்து அவற்றின் வாயிலாக பயன் அடைதல்.	L1 - நினைவில் கொள்ளுதல்
TEXTBOOKS: தமிழ் இலக்கிய வெளியீடுகள் புத்தகங்கள்		
1.	தமிழ் இணைய கல்விக்கழகம் (Tamil Virtual University) - www.tamilvu.org.	
2.	தமிழ் விக்கிப்பீடியா (Tamil Wikipedia) -https://ta.wikipedia.org.	
3.	தர்மபுர ஆதீன வெளியீடு.	
4.	வாழ்வியல் களஞ்சியம் - தமிழ்ப் பல்கலைக்கழகம், தஞ்சாவூர்.	
5.	தமிழ்க்கலைக்களஞ்சியம் - தமிழ் வளர்ச்சித்துறை (thamilvalarchithurai.com).	
6.	அறிவியல் களஞ்சியம் - தமிழ்ப் பல்கலைக்கழகம், தஞ்சாவூர்.	

Note:
Syllabus for the courses offered from 3rdSemester to4th Semester, will be added after the approval of the Board of Studies (BoS) & Academic Council (AC) in due course.