Faculty Profile

A1	Personal Details

K.Rajesh, B.E., M.E.,

S/o K.Kandasamy

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A2	Areas of Interest	VLSI Design, Testing of Digital Circuits and Artificial Intelligence

A3	Subjects Taught	
UG		**UG**
Digital Electronics		Advanced Microprocessor and Microcontroller
Electronic Devices		Wireless Communication
VLSI Design		
Electronic Circuits – I		**PG**
Electronic Circuits – II		Testing of VLSI Circuits
Linear Integrated Circuits		Analysis and Design of Analog ICs
Microprocessor and Microcontroller		CAD for VLSI Circuits
Advanced Microprocessor		VLSI Design Techniques
Analog and Digital Communication		Advanced Microprocessor and Microcontroller

A4	Academic Background			
Degree	**Specialization**	**Name of the Institute**	**University**	**Month & Year of Passing**
M.E.	VLSI Design	Bannari Amman Institute of Technology, Sathyamangalam	Anna University, Coimbatore	May - 2011
B.E.	Electronics and Communication Engineering	Sona College of Technology, Salem	Anna University, Chennai	May - 2008
12th	-	Vidhyaa Vikash Higher Secondary School	Matriculation	April - 2004
10th	-	Mahendra Matriculation Higher Secondary School	Matriculation	April - 2002

A5	Work Experience						
Name of the Institution		**Position**		**From**		**To**	
Knowledge Institute of Technology, Salem		Assistant Professor		May 2011		May 2021	
Total Experience	10 Years	**Teaching**	10 Years	**Research**	-	**Industry**	-

A6	Roles and Responsibilities
1.	NBA coordinator for Department of ECE
2.	NAAC coordinator for Department of ECE
3.	Admission Incharge for Department of ECE
4.	Faculty Incharge for Pacific (VLSI Design) Club
5.	Faculty Incharge for IEEE Blended Learning Program for VLSI
6.	Class Advisor

A7	Memberships in Professional Bodies
S.No.	**Name of the Professional Body**
1.	Life member of Indian Society for Technical Education (ISTE) (No : LM107416)
2.	Life member of Engineering Professional Society

A8	Programs Organised
1.	Organized two week ISTE STTP on "CMOS, Mixed Signal and Radio Frequency VLSI Design in association with Indian Institute of Technology, Kharagpur from 30th January, 2017 to 4th February, 2017.
2.	Organized two day Hands on Training on "**Digital VLSI Design"** during 27th & 28th January 2016.
3.	Organized Three days Non Formal Course on "**Hands on Training on Mentor Graphics EDA tools**" during 21st – 23rd December 2015.
4.	Organized one day Guest Lecture on "**VLSI Design Techniques**" on 27th August 2015.
5.	Organized Three days Non Formal Course on "**Digital VLSI Design**" during 11th – 15th December 2015.
6.	Organized one day workshop on "**LabVIEW Based FPGA Design**" on 28th August 2014.
7.	Organized one day IEEE sponsored workshop on "**VLSI for Wireless Communication**" on 12th August 2014.
8.	Organized one day workshop on "**Designing ICs using Fedora Electronics Lab**" on 22nd April 2014.

9.	Organized one day Guest Lecture on "**Research Issues in Low Power VLSI Design**" on 12th March 2014.
10.	Organized one day workshop on "**Analysis and Design of Analog VLSI Design**" on 14th February 2014.
11.	Coordinated AICTE sponsored two days national level seminar on "Intellectual **Key for Industrial Applications using Embedded System**" during 25th & 2th September 2013.
12.	Organized one day IEEE sponsored workshop on "**Role of ICs in Leveraging Green Technologies"** on 19th October 2013.
13.	Coordinated two days IEEE sponsored national seminar on "**Research Challenges in Signal Processing**" during 3rd & 4th April 2012.

A9	**Highlights of Major Contributions**
1.	Involved in writing proposal for seminar and received fund of 1 Lakhs from AICTE for conducting National level Seminar.
2.	Guided Student projects and received cash prizes from Texas Instruments and other Project Competitions.
3.	Coordinated and Organized various programs in VLSI Technical club.
4.	Acted as Reviewer for the book Electronic Devices (McGraw Hill Education (India) Pvt. Ltd.) for the year 2016

A10	**Training Programmes Attended**
1.	Two week Faculty Development Program on "**Pedagogy for Online and Blended Teaching Learning Process**" conducted by Indian Institute of Technology, Bombay from 14th September, 2017 to 12th October, 2017.
2.	Two week Faculty Development Program on "**Foundation Program in ICT for Education**" conducted by Indian Institute of Technology, Bombay from 3rd August, 2017 to 7th September, 2017.
3.	One week ISTE STTP for coordinators on "**CMOS, Mixed Signal and Radio Frequency VLSI Design**" conducted by Indian Institute of Technology, Kharagpur from 19th September, 2016 to 23rd September, 2016.
4.	One week Didactic Workshop on **"Electronics System Design, Manufacturing and Testing"** organized by the Department of Electronics and Instrumentation Engineering at BMS College of Engineering, Bangalore in association with Entuple Technologies during 27th - 31st July 2015.
5.	Three days Faculty Development Programme on **""** organized by the Department of MBA at American University of India, Kodaikanal during 20th – 22nd May 2015.
6.	Five days Workshop on **"Mission10X – UTLP Expert"** conducted by Wipro Technologies, Bangalore during 19th – 23rd January 2015.
7.	Two Week ISTE Workshop on **"Control Systems"** conducted by Indian Institute of Technology, Kharagpur at Knowledge Institute of Technology, Salem during 2nd – 12th December 2014.

8.	Two day ISTE e-seminar on **"Steps 2 Research"** organized by Department of Computer Science, Department of Computer Applications, Amal Jyothi College of Engineering, Kanjirappally in association with ISTE Kerala Section and CSI Cochin Chapter during 19th – 20th September 2014.
9.	Two Week ISTE Workshop on **"Signals and Systems"** conducted by Indian Institute of Technology, Kharagpur at Knowledge Institute of Technology, Salem during 2nd – 12th January 2014.
10.	Five days Short term course on **"Advances in VLSI Signal Processing"** offered by Department of Electronics and Electrical Communication Engineering at Indian Institute of Technology, Kharagpur during 3rd – 7th December 2013.
11.	Three days Faculty Development program on **"Teaching and Learning"** conducted at Knowledge Institute of Technology in association with Wipro Technologies, Bangalore during 23rd – 25th September 2013.
12.	Two weeks AICTE sponsored Faculty Development Programme on **"Hands on Training on Design Finishing for Chip Tapout"** organized by Department of Electronics and Communication Engineering at R.M.K Engineering College during 17th – 29th June 2013.
13.	Two Week ISTE Workshop on **"Analog Electronics"** conducted by Indian Institute of Technology, Kharagpur at Knowledge Institute of Technology, Salem during 4th – 14th June 2013.
14.	Two days Workshop on **"Frontend and Backend ASIC Design using Synopsys EDA Tools"** organized by Department of Electronics and Communication Engineering at K.S.Rangasamy College of Technology, Tiruchengode during 1st – 2nd March 2013.
15.	Two day ISTE Workshop on **"Aakash for Education"** conducted by Indian Institute of Technology, Kharagpur at Knowledge Institute of Technology, Salem during 10th – 11th November 2012.
16.	One day Workshop on **"Reconfigurable Technology and its Applications"** organized by Department of Electronics and Communication Engineering at Sona College of Technology, Salem in association with Enixs Technology, Trichy on 29th October 2011.
17.	Two day Workshop on **"FPGA Based VLSI Design"** organized by Department of Electronics and Instrumentation Engineering at Kongu Engineering College during 16th – 17th September 2011.

A11	**Special Lectures Presented**
1.	Handled two day workshop on "**Hardware Modelling of HDL using UTLP (Spartan 6 FPGA)** Kit", organized by Department of Electrical and Electronics Engineering at Knowledge Institute of Technology, Salem during 14th – 15th September 2015.
2.	Handled two day Hands on Training on "**Hardware Modelling with HDL using Spartan 3E FPGA kit**" , Organized by Department of Electronics and Communication Engineering at Knowledge Institute of Technology, Salem during 31st August and 1st September, 2015.

3.	Handled one day Hands on Training on "**Xilinx 12.1 Simulation Software**" , Organized by Department of Electronics and Communication Engineering at Knowledge Institute of Technology, Salem during 17th August 2015.
4.	Handled a IEEE SB MAS Sponsored one-day workshop on **"Prominence of EDA Tools"** organised by Department of Electronics and Communication Engineering at Knowledge Institute of Technology, Salem during 3rd July 2015.
5.	Handled Three days Non Formal Course on "**Digital VLSI Design"** organized by Department of Electronics and Communication Engineering at Knowledge Institute of Technology, Salem during 11th – 15th December 2014.

A12	**Awards**
1.	Received Young Faculty Achiever (YFA–2018) award from Engineering Professional Society for academic excellence
2.	Received achiever award (2016) from college for Mentoring students Projects and won Prizes at various events.
3.	Received achiever award (2014) from college for efficient support in getting Rs 1 Lakh fund from AICTE to conduct National Level seminar.

A13	**Research Publications**				
Total Number of Publications	**International Journal**	**National Journal**	**International Conference**	**National Conference**	**Total**
	9	4	11	11	35
Publications (Journals)					
1.	R.Hemalatha, **K.Rajesh**, M.Shenbagapriya and N.Santhiyakumari, Fabric Defects Detection and its Implementation in TI-OMAP, Journal of Electronics and Communication Systems, Vol.2, No.1, Page 1-6 © MAT Journals, 2017				
2.	S.Suvarna, **K. Rajesh** and T. Radhu, "Design and Implementation of Radix-4 Booth Multiplier with Adaptive Hold Logic", International Journal of Innovative Research in Science, Engineering and Technology, Vol.3, No.1, pp.66-72, 2016.				
3.	K.Arvind, K.Hemadarshini, S.Indhuja. S.Ramkumar and **K.Rajesh**, "A Robotic ARM based chess board for visually challenged people", International Journal of Advanced Research in Management Architecture Technology & Engineering, pp. 280-286, 2016				
4.	S.Suvarna, **K. Rajesh** and T. Radhu, "A Modified Architecture for Radix-4 Booth Multiplier with Adaptive Hold Logic", International Journal of Students' Research In Technology & Management, Vol.4, No.1, pp. 01-05, 2016.				
5.	S.Suvarna, **K. Rajesh** and S.Veerakumar, "A modified Multiplier Architecture design Adaptive hold logic and Razor flip flop", International Journal of Emerging Trends in Science and Technology, Vol.03, No.03, 2016.				
6.	S.Suvarna, **K. Rajesh** and S.Veerakumar, "Aging Aware Radix-4 Booth Multiplier with Adaptive holds logic and Razor flip flop", I-Manager's Journal on Electronics Engineering, Vol.6, No.1, pp. 13-20, 2015.				

7.	S.Suvarna, **K. Rajesh** and C.Gomathi, "Petrochemical Level Indicator and Controller for Automation Industries using UTLP kit", International Journal of Innovative Research in Science, Engineering and Technology, Vol.4, No.6, pp:806-813, 2015.
8.	S.B.Abirami, K.Manoj, C.Maruthu Pandian and **K.Rajesh**, "Analysis of Self Checking Additional Adder circuit in Combinational Circuits", Journal for Research in Applied Science and Engineering Technology, Vol.3, No.3, pp:768-775, 2015.
9.	R.Mohanapriya and **K.Rajesh**, "Modified Architecture of Multiplier and Accumulator using Spurious Power Suppression Technique", International Journal of Students' Research In Technology & Management, Vol.3, No.2, pp: 258-263, 2015.
10.	R.Mohanapriya and **K.Rajesh**, "A Modified Architecture of Multiplier and Accumulator using Radix 4 Modified booth Algorithm", I-Manager's Journal on Circuits and Systems, Vol.02, No.04, pp:1-6, 2014.
11.	K.Sahithiya, A.Mohanapriya, S.Kannan and **K.Rajesh**, "FPGA Implementation of Low Power and High Speed Multiplier", International Journal for Scientific Research and Development, Vol.3, No.1, pp: 258-263, 2014.
12.	Dr.N.Santhiyakumari, C.Babu, C.Gomathi, **K.Rajesh** and M.Shenbagapriya, "A Novel Approach for Quality Education towards Industry Expectations", I-Manager's Journal on Educational Technology, Vol.11, No.1, pp: 7-14, 2014.
13.	R.Tamilmani, **K.Rajesh**, Dr.N.Santhiyakumari, "Modified Divide by 2/3 Counter Design Using MTCMOS Techniques", I-Manager's Journal on Electronics Engineering, Vol.4, No.2, pp:22-27, 2014
Publications (Conferences)	
14.	S.Suvarna, **K.Rajesh** and C.Gomathi, "Petrochemical Level Indicator and Controller for Automation Industries using UTLP Kit", International Conference on Multicon'15, Vol. 02, pp. 354 – 361, April 2015.
15.	S.Suvarna, **K.Rajesh** and T. Radhu, "A Modified Architecture for Radix-4 Booth Multiplier with Adaptive Hold Logic", International Conference on Electrical, Electronics, Information and Computational Applications, pp. 52 – 53, March 2015.
16.	S.Suvarna and **K.Rajesh**, "A Modified Multiplier Architecture Design with Adaptive Hold Logic and Razor Flip Flop", International Conference on Breakthrough in Engineering, Science and Technology, pp:163 – 168, March 2016.
17.	R.Mohanapriya and **K.Rajesh**, "A Modified Architecture of Multiplier and Accumulator using Spurious Power Suppression Technique", International Conference on CONFLUENCE V2, Jan-15
18.	R.Mohanapriya, **K.Rajesh** and P.S.Sudarshana, "VLSI Implementation of Multiplier and Accumulator Architecture using Radix -4 Modified Booth Algorithm", IEEE sponsored 2nd International Conference on Innovations in Information Embedded and Communication Systems, Vol.7, pp: 258-263, March 2015.
19.	S.B.Abirami, K.Manoj, C.Maruthu Pandian and **K.Rajesh**, "Analysis of Self Checking Additional Adder circuit in Combinational Circuits", International Conference on Recent Innovations in Engineering and Technology, pp: 1-5, March 2015.
20.	K. Nehru, A. Shanmugam, P. Gowthaman and **K.Rajesh**, "Efficient parallel Multiplier and Accumulator Architecture for High Speed Arithmetic Operations", International Conference on Advances in Engineering and Technology, 2011.

21.	Tamilmani.R, **K.Rajesh** and Dr.N.Santhiyakumari, "Modified Divide by 2/3 Counter Design using MTCMOS Techniques", International Conference on Recent Innovations in Engineering, 2014
22.	Saranya.M and **K.Rajesh**, "Time Optimization in RTL circuits using VHDL", International Conference on Recent Innovations in Engineering, 2014
23.	Sahithiya.K, Mohanapriya.A, Kannan.S and **K.Rajesh**, "FPGA Implementation of Low Power and High Speed Mixed Architecture Multiplier", International Conference on Competency Building Strategies in Business and Technology, Vol.2, March 2015.
24.	K.Jayalakshmi, K.Prem Kumar, M.Suriya Prabha, and **K.Rajesh**, FPGA Implementation of Mixed Architecture Multiplier for Power Optimizing Techniques International Conference on Competency Building Strategies in Business and Technology, Vol.2, March 2015.

A14	**Project Guidance**
	UG
1.	Accident Prevention System in Train Wreck
2.	FPGA Implementation of Analysis of Self Checking Additional adder in Combinational Circuits.
3.	FPGA Implementation of Mixed Architecture multiplier for power optimizing technique
4.	FPGA Implementation of Low Power and High Speed Mixed Multiplier Architecture
5.	Automatic Rotation Camera based on human position and Speaker Voice.
6.	Automatic Irrigation System
7.	Smart Blood Stockpile for Victims
	PG
8.	Aging Aware Radix-4 Booth Multiplier with Adaptive Hold
9.	Enhancement of validation test sets to improve the performance of test generation using VHDL
10.	Modified Divide by 2/3 counter design using MTCMOS technique
11.	A Modified Architecture of Multiplier and Accumulator using Spurious Power Suppression Technique